

What is claimed is:

1. A method of controlling light sensitive elements arranged in rows and columns in an image sensor for a roller shutter sensing sequence and wherein the elements are double sampled comprising the steps of:
 - a. initially resetting a light sensitive element during a reset time t_{RESET} ;
 - b. reading the light sensitive element after an integration time t_{INT} during a read time t_{READ} ; and
 - c. resetting the light sensitive element a second time during a portion of the read time t_{READ} .
2. A method as claimed in claim 1 wherein the light sensitive elements are CMOS pixels.
3. A method as claimed in claim 2 wherein the CMOS pixels are three transistor pixels.
4. A method as claimed in claim 1 wherein step a. includes:
 - a.1 resetting the light sensitive elements in each row simultaneously; and
 - a.2 sequentially resetting each successive row of light sensitive elements after a time period t_{ROW} .
5. A method as claimed in claim 4 wherein $t_{\text{ROW}} \geq t_{\text{READ}}$.
6. A method as claimed in claim 4 wherein $t_{\text{ROW}} \geq (t_{\text{READ}} + t_{\text{HB}})$ where t_{HB} is horizontal blank time.
7. A method as claimed in claim 4 wherein the second resetting time occurs towards

the end of the read time t_{READ} .

8. An apparatus for controlling light sensitive elements arranged in rows and columns in an image sensor for a roller shutter sensing sequence wherein the elements are double sampled comprising:
 - element reset signal producing means;
 - initial reset means for controlling the element reset signal producing means to produce an initial reset signal;
 - element access signal producing means; and
 - double sample control means responsive to the element access signal producing means for controlling the element reset signal producing means to produce a second reset signal.

9. An apparatus for controlling light sensitive elements arranged in rows and columns in an image sensor for a roller shutter sensing sequence wherein the elements are double sampled, comprising:
 - element reset signal producing means for elements in a row;
 - initial reset means for controlling the element reset signal producing means to produce an initial reset signal for the elements in the row;
 - access signal producing means for the elements in the row; and
 - double sample control means responsive to the access signal producing means for controlling the reset signal producing means to produce a second reset signal for the elements in the row.

10. Apparatus as claimed in claims 8 or 9 wherein the light sensitive elements are CMOS Pixels.

11. Apparatus as claimed in claims 8 or 9 wherein the light sensitive elements are

three transistor CMOS Pixels.

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12. An apparatus for controlling light sensitive elements arranged in rows and columns in an image sensor for a roller shutter sensing sequence wherein the elements are double sampled, comprising:
- a reset control circuit for providing reset signals to at least one light sensitive element in a row;
 - a reset decode circuit for activating the reset control circuit to provide an initial reset signal to the at least one light sensitive element in the row;
 - 10 - a row access decode circuit for providing a row access signal to the at least one light sensitive element in the row; and
 - a double sample control circuit having an input coupled to the row access decode circuit and an output coupled to the reset control circuit for activating the reset control circuit to provide a second reset signal to the at least one light sensitive element in the row.
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13. An apparatus as claimed in claim 12 wherein the light sensitive elements are CMOS pixels.
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14. An apparatus as claimed in claim 13 wherein the light sensitive elements are three transistor CMOS pixels.
15. An apparatus as claimed in claim 13 wherein the reset control circuit, the reset decode circuit and the double sample control circuit are NAND gates and the row access decode circuit is an AND gate.
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16. An apparatus as claimed in claim 13 which further comprises:
- a reset driver coupled to the reset control circuit for generating the reset signals; and

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17. An apparatus as claimed in claim 16 wherein the reset driver and the row access drivers are non-inverting amplifiers.